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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,300	09/17/2003	Rajendran Nair	042390.P8667C	6195
7590	12/01/2004		EXAMINER	
Michael J. Mallie BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP Seventh Floor 12400 Wilshire Boulevard Los Angeles, CA 90025			NGUYEN, LONG T	
			ART UNIT	PAPER NUMBER
			2816	
			DATE MAILED: 12/01/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/665,300	NAIR, RAJENDRAN	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
 THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 07 September 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-4,6-9 and 11-25 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1,4,6-9,11-19 and 21-25 is/are rejected.
 7) Claim(s) 2,3 and 20 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 17 September 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date: _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date: _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on 9/7/04 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 6,717,445 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the positive input of the first amplifier is coupled to the input signal through a first output level based buffer impedance modulator circuit and the positive input of the second amplifier is coupled to the input signal through a second output level based buffer impedance modulator circuit in claim 3 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Note that the drawings does not show the first and second based buffer impedance modulator circuits.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement

Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 1-4, 6-9, 12 and 21 are objected to because of the following informalities:
 - Claim 1, lines 2, 3 and 7, "to receives" needs to be changed to --coupled to receive--.
 - Claims 2-4 and 6-9 are objected to because they include the informalities of claim 1.
 - Claim 4, line 1-2, "the voltage following circuit comprises" needs to be deleted because independent claim 1 already recited that the voltage following circuit comprises the first and second transistors.

Claim 12, line 1, "claim 13" needs to be change to --claim 11--.
Claim 21, line 1-2, "the voltage following circuit comprises" needs to be deleted because independent claim 19 already recited that the voltage following circuit comprises the first and second transistors.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
5. Claims 4, 21 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 4 and 21, the recitation “the gate being coupled to receive the input signal” on lines 3 and 7 is indefinite because it is misdescriptive since it is inconsistent with the independent claims 1 and 19, respectively, since the claims 1 and 19 clearly recited that the voltage following circuits including a first transistor coupled to a first amplifier, and a second transistor coupled to the second amplifier. It is clearly from Figure 6 that the gates of the first and transistors coupled to the output of the first and second amplifiers, respectively (i.e., the gates of the first and second transistors does not coupled to receive the input signal). Thus, it appears that “the gate being coupled to receive the input signal” on lines 3 of these claims need to be changed to --the gate being coupled to an output of the first amplifier--, and “the gate being coupled to receive the input signal” on line 7 of these claims needs to be changed to --the gate being coupled to an output of the second amplifier--.

With respect to claim 24, the recitations “generating the high output signal includes instructions to generate the high output signal substantially independent of power supply noise” and “for generating the low output signal includes instructions to generate the low output signal substantially independent of power supply noise” are indefinite because they are misdescriptive. Note that, line 20 of page 6 of the instant specification only discloses that output signal 305 will be less depend on the power supply and more depend on the input signal 301. Thus, the specification does not specifically disclose that it is independent of power supply noise.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 4, 6-9, 11-19 and 21-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaplinsky (USP 5,488,322).

With respect to claims 1, 4, 6-9, 11-19 and 21-25, the Kaplinsky reference discloses processing system (Figure 5) comprising a circuit (Figure 5), wherein the circuit (Figure 5) includes: a signal input (52) to receive a signal (IN); a buffer circuit (73) to receive the input signal (IN) and to generate a buffer circuit output (46); and a voltage following circuit (41, 43, 45, 47) comprising a first amplifier (41) couple to a first transistor (45) and a second amplifier (43) coupled to a second transistor (47), wherein the voltage following circuit receiving the signal (IN) and to generate a voltage following output (46) wherein the buffer circuit output and the voltage following circuit output are coupled to a circuit output node (46). Note that, the circuit (Figure 5) is an interface, so it is reasonable to consider the circuit (Figure 5) as a repeater or buffer, and that the circuit is capable of being used in a signal distribution system or a large scale integrated circuit. Note, with claim 22, because the circuit is implemented, so it is inherent that the disk or hard-drive that store the netlisted file of the circuit which is used to simulate the circuit when design is the machine-readable medium having stored thereon instruction.

Note, insofar as understood in claims 4 and 21, the first transistor (45) comprising an NMOS transistor having the gate coupled to the output of the first amplifier (41), and the second transistor (47) having the gate coupled to the output of the second amplifier (43). See Col. 4, lines 16-20.

Note with respect to claims 12, 16 and 23, it is seen in the operation of Figure 5 that the voltage following circuit includes means (45) for generating a logic high output signal when the input signal (IN); and means (47) for generating a logic low output signal when the input signal is low because when the input signal (IN) is low (see line 59 of Col. 3 to line 15 of Col. 4).

Note with respect to claims 13, 17 and 24, because the structure of the prior art (Figure 5) is fully met, and that the operation of the circuitry (Figure 5) depends on the input signal (IN) and the Kaplinsky reference does not specifically recited that the circuitry depends on the power noises, so it is reasonable to consider that the operation of the circuitry more dependence on the input signal and less dependence on the power supply noise.

Note with respect to claims 14, 18 and 25, Figure 5 shows that the buffer circuit (73) includes a first inverter and a second inverter.

Allowable Subject Matter

8. Claims 2, 3 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2 and 20 would be allowed because the prior art of record fails to disclose or suggest all the limitations of these claims. In particular, the prior art of record fails to disclose, in combination with other limitations, the voltage following circuit (706, 708, 702, and 704 in Figure 6) which includes a first amplifier (706, Figure 6), an NMOS transistor (702, Figure 6), a second amplifier (708, Figure 6) and a PMOS transistor (704, Figure 6) with the recited connection set forth in these claims.

Claim 3 would be allowed because it depends on claim 2.

Response to Arguments

9. Applicant's arguments filed on 9/7/04 have been considered but are moot in view of the new ground(s) of rejection.

Note that Applicant does not address the objection to the drawings and the indefinite problem of claim 24 indicated in the last office action. Thus, the objection to the drawings and the rejection of claim 24 under 35 U.S.C. 112, 2nd paragraph are repeated in the office action. Note that applicant's amendment also necessitated the rejection of claims 4 and 21 under 35 U.S.C. 112, 2nd paragraph.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 18, 2004



Long Nguyen
Primary Examiner
Art Unit: 2816